# GSM/DCS1800/PCS1900 Baseband Processing Chipset

# AD20msp415

## FEATURES

**Complete Baseband Processing Chipset Performs:**
- Speech Coding/Decoding (GSM 06.XX)
- Channel Coding/Decoding (GSM 05.03)
- Equalization with 16-State Viterbi, Soft Decision
- All ADC and DAC Interface Functions
- Includes All Radio, Auxiliary and Voice Interfaces

**Support for GSM Data Services**
**Embedded 16-Bit Microcontroller**
**Embedded 16-Bit DSP**
**Integrated SIM and Keyboard Interface**
**Interface to AD6430 GSM RF Chipset**
**Interface to EFR Coprocessor**
**JTAG Boundary Scan**
**Layer 1 Software Provided with Chipset**
**Software Compatible with AD20msp410**
**Full Phase 2 Protocol Stack Software Available**
**Full Reference Design Available for**
- Baseband Section and Radio Section

**Ultralow Power Design**
- 2.7 V to 3.3 V Operating Voltage
- Intelligent Power Management Features
- XXX mW Power Dissipation in Talk Mode
- XX mW Power Dissipation in Standby Mode

**Two TQFP Devices, Occupying Less than 7.5 $cm^2$**

## APPLICATIONS

**GSM/DCS1800/PCS1900 Mobile Radios**

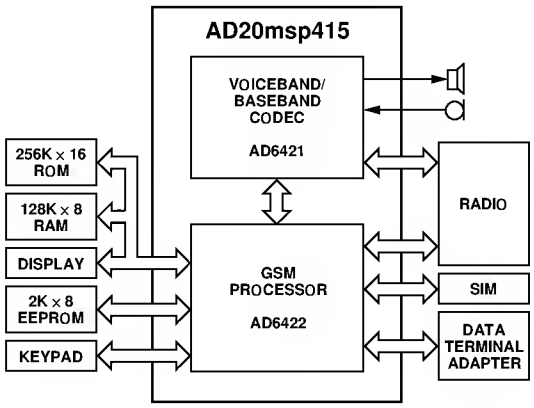
## GENERAL DESCRIPTION

The Analog Devices GSM Baseband Processing Chipset provides a competitive solution for GSM based Mobile Radio Systems. It is designed to be fully integrated, easy to use, and compatible with a wide range of product solutions. Examples are GSM 900, DCS1800, PCS1900 handsets and PCMCIA data cards. The AD20msp415 is the higher integrated successor of the AD20msp410 chipset, which passed European GSM Type Approval in June, 1996.

The chipset consists of two highly integrated, sub-micron, low power CMOS components that perform the entire baseband signal processing of the GSM handset. The system architecture is designed to be easily integrated into current designs and form the basis for next generation designs.

The chipset uses an operating supply voltage of 2.7 V to 3.3 V which, coupled with the extensive power management features, significantly reduces the drain on battery power and extends the handsets talk time and standby time.

## SYSTEM ARCHITECTURE




## CHIPSET COMPONENTS

### GSM Processor (GSMP)

The AD6422 combines application specific hardware, an embedded 16-bit DSP and an embedded 16-bit microcontroller (Hitachi H8/300H). It performs channel coding and decoding and executes the protocol stack and user software. The DSP implements full rate speech transcoding according to GSM specifications, including Discontinuous Transmission (DTX) and Comfort Noise Insertion (CNI). A high performance soft-decision Viterbi equalizer is also implemented in software embedded in the DSP. The embedded microcontroller executes the Layer 1, 2, 3 and user MMI software. The required Layer 1 software is supplied with the chipset. To ensure minimum power consumption, the GSMP has been designed to control all the power-down functions of the other components in the handset.

### Voiceband/Baseband Converter (VBC)

The AD6421 performs the voiceband and baseband analog-to-digital and digital-to-analog conversions, interfacing the digital sections of the chipset to the microphone, loudspeaker and radio section. In addition, the VBC contains all the auxiliary converters for burst-ramping, AFC, AGC, battery and temperature monitoring. The chipset interfaces directly with the radio and supplies all the synthesizer and timing control signals required to support two synthesizers and a variety of radio architectures including the AD6450 GSM RF-Chipset.

### Software

The required Layer 1 software is supplied with the chipset. In addition, an object code license is available for Layers 2 and 3 of the protocol stack.

REV. 0



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## ARCHITECTURE OVERVIEW

Analog Devices and The Technology Partnership (TTP) provide a cost effective and proven method of attaining the baseband processing subsystem and protocol stack software. This data sheet includes functional descriptions of the baseband processing subsystem and the Protocol Stack Layer 1. The Technology Partnership can provide licenses to software and reference designs in all areas of a GSM handportable terminal.

For detailed information about the individual chipset components, please refer to the AD6421 (VBC) and AD6422 (GSMP) data sheets for electrical characteristics and timing information.

## FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the GSM baseband processing chipset. The chipset can be viewed as a functional block that contains a number of discrete functional units. The electrical and functional interfaces to the rest of the system are briefly described at the end of this section and described in detail in the individual data sheets for each component.

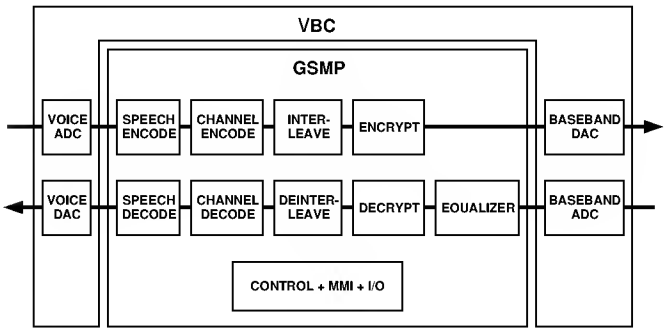


*Figure 1. Functional Block Diagram*

### Uplink

The uplink baseband processing functions include the following operations:

#### Analog-to-Digital Voice Conversion (VBC)

A conventional microphone, connected directly to the VBC, provides an analog input signal to the ADC. The analog voice signal is sampled at 8 kHz, producing 13-bit linear values corresponding to the magnitude of the input. The ADC includes all required filtering to meet the GSM specifications. The sampled voice data is passed to the GSMP through a dedicated serial port.

#### Speech Encoding (GSMP)

The GSMP receives the voice data stream from the VBC and encodes the data from 104 kb/s to 13 kb/s. The algorithm used is Regular Pulse Excitation, with Long Term Prediction (RPE-LTP) as specified in the 06-series of GSM Recommendations.

#### Channel Coding (GSMP)

The information received from the speech coder contains parameters that have different levels of priority. These are protected to different levels within the channel coding. The encode protection process incorporates block coding and convolutional encoding. In addition to the normal speech traffic channels, the channel coding function also supports data transmission at full rate and half rate. After the interleave process (if necessary) the data is encrypted using the required A5/1 or A5/2 encryption algorithm. Data is then formatted into bursts, with the required timing and training sequences, and sent to the VBC through a dedicated serial port.

#### GMSK Modulation and D/A Conversion (VBC)

The VBC receives data at 270 kb/s. The VBC uses an on-chip lookup table to perform GMSK modulation. A pair of 10-bit matched differential DACs convert the modulated data and pass I and Q analog data to the transmit section of the radio subsystem.

### Downlink

The downlink baseband processing functions include the following operations:

#### Analog-to-Digital Conversion (VBC)

The receiver I and Q signals are sampled by a pair of ADCs at 270 kHz. The I and Q samples are transferred to the GSMP through a dedicated receive path serial port.

#### Equalization (GSMP)

The equalizer recovers and demodulates the received signal and establishes local timing and frequency references for the mobile unit as well as RSSI calculation. The equalization algorithm is a version of the Maximum Likelihood Sequence Estimation (MLSE) using the Viterbi algorithm. Two confidence bits per symbol provide additional information about the accuracy of each decision to the channel codec's convolutional decoder. The equalizer outputs a sequence of bits including the confidence bits.

#### Channel Decoding (GSMP)

Data is decrypted as required, using the A5/1 or A5/2 decryption algorithm prior to the deinterleave process. The deinterleave process is an exact inversion of the interleave process used by the transmit section. The decode function then performs convolutional decoding and parity check. The convolutional decoder uses a Viterbi algorithm, with two soft decision confidence bits supplied by the equalizer. Error control mechanisms are used to ensure adequate bad frame indication.

#### Speech Decoding (GSMP)

Encoded speech data is transferred at 20 ms intervals in blocks of 260 bits plus the Bad Frame Indicator (BFI). The speech decoder supports a Comfort Noise Insertion (CNI) function that inserts a predefined silence descriptor into the decoding process. The GSMP also implements control of talker side-tone and short term echo cancellation. The resulting data, at 104 kb/s, is transferred to the VBC through a dedicated serial path.

#### Voice Digital-to-Analog Conversion (VBC)

The Voice DAC function of the VBC operates at 8 kHz and includes all the needed filtering. The analog signal can be controlled in volume and directly drive a small earpiece as well as a separate auxiliary output.

## AUXILIARY SYSTEM FUNCTIONS

The GSMP and the VBC perform a number of auxiliary functions that are essential to build a complete mobile radio.

A general radio section constitutes the three functions of transmitter, receiver and synthesizer. Figure 2 shows how the baseband chipset interfaces to a typical radio architecture. The transmitter is fed with baseband analog I and Q signals from the VBC and upconverted to 900 MHz for GSM applications and 1800 MHz for PCN applications.

A dedicated power amplifier increases the RF signal to the required level. The receiver amplifies the antenna signal, down-converts it to an intermediate frequency (IF) and amplifies it there again. After second conversion to baseband the I and Q components of the signal are fed into the VBC.

The three auxiliary functions, AGC, AFC and Power Ramping are included to interface to the radio section.

### Power Ramp Envelope

To meet the spectral and time-domain specifications of the transmitted output signal, the burst has to follow a specified power envelope. The envelope for the power profile originates in the GSMP as a set of coefficients, down-loaded and stored in the VBC. This envelope profile is fed to the RAMP DAC on the VBC with each burst. The analog output is fed into the RF power amplifier, controlling the power profile and absolute level of the transmitted data. The power control loop of the power amplifier can also feedback an error control signal that indicates whether the output functions are out of specification and the radio can be switched off accordingly.

### Automatic Gain Control (AGC)

The mobile radio has to cope with a wide range of input signal levels. The major part of the overall gain is provided in the IF amplifier. The incoming signal level is analyzed in the GSMP and a digital gain control signal is sent to the VBC. The AGC DAC generates the appropriate analog control signal for the IF amplifier.

### Automatic Frequency Control (AFC)

The mobile radio tracks the master clock provided by the base station to compensate for temperature/frequency drifts in the crystal oscillator. Drift of the crystal oscillator over time and temperature has to be compensated as well as frequency shifts due to the Doppler effect in the case of a moving mobile radio. The received signal is analyzed in the GSMP and a digital control signal is generated. This signal is sent to the AFC DAC in the VBC to control the voltage controlled, temperature compensated crystal oscillator (VCTCXO).

### Synthesizer Control

The GSMP and the respective parts of the Layer 1 software control the overall timing and frequency generation of the radio subsystem. This includes control signals for two synthesizers, power-down control signals and power amplifier monitor signals. Detailed information can be found in the AD6422 data sheet.

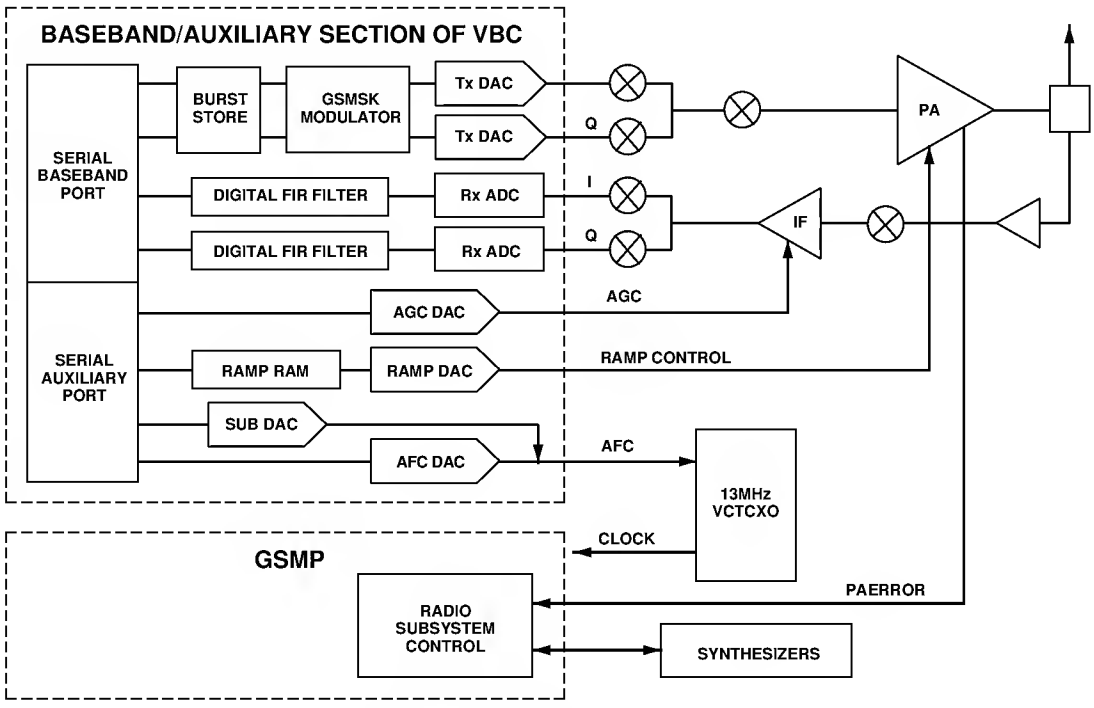


*Figure 2. Control of Radio Subsystem*

**Generation of Auxiliary Audio Signals**

Under control of Layer 1, the GSMP can generate a variety of fixed and user-programmable tones. This includes all standard DTMF and Call Progress tones as well as user defined tones. The tone structure can consist of up to four frequency components with individual durations. The GSMP also generates Talker Sidetone as specified in the GSM recommendations. In comparison to traditional hardware implementations, this software implementation provides manufacturing flexibility over a wide range of speaker/microphone sensitivities.

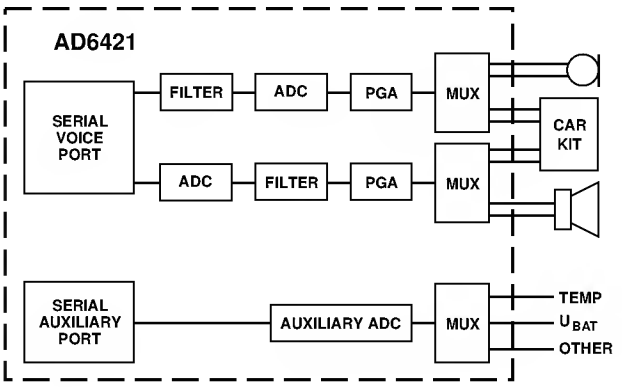


*Figure 3. Audio/Auxiliary Section of the AD6421*

Figure 3 shows the audio section and the auxiliary ADC of the VBC. Input signals can come from either a directly connected microphone or from a remote microphone in a car kit. Input gain can be set to 0 dB or +26 dB. The output signal can be directly connected to a small earpiece and, for further amplification, to an external car kit. The output PGA can be programmed for –15 dB or +6 dB.

## DATA SERVICES

Data Services is considered to be an essential feature for GSM terminals and the AD20msp415 chipset is designed to provide flexible and low cost implementation of Data Services supported via the GSM air interface.

The selected system architecture shown in Figure 4 provides for minimum terminal Bill of Materials, the lowest possible number of interconnection points and the lowest power consumption when running speech traffic only. The GSMP performs full channel coding and decoding for TCH/F9.6, TCH/F4.8 and TCH/F2.4 data rates. The interface to the chipset is a user-configurable, 3-wire synchronous or asynchronous serial interface supplying V110′ data packets as defined in GSM 05.03, combined with protocol information and control to the Application Layer.

External to the terminal is the Data Terminal Adapter (DTA) that runs the Data Services Software. Included in the DTA are the rate adaptation functions and the Data Services application.

The Command Interpreter resident on the mobile supports a serial interface protocol with the DTA by which both traffic data and control information are communicated.

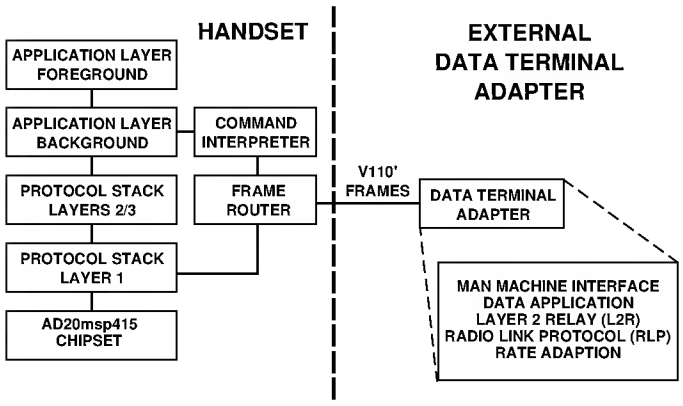


*Figure 4. Implementation of Data Services*

## SOFTWARE IMPLEMENTATIONS

A full implementation of the GSM Layer 1 functionality is supplied as an object code module, for execution on the controller, embedded in the GSMP. Functions performed by this software include:

- Initial scan of GSM/E-GSM/PCN band and selection of strongest thirty channels as required by 03.22 and 05.08.
- Mobile oscillator adjustment, timing synchronization and BCCH decoding from serving cell (camping-on).
- Base station frequency and timing measurements and BSIC extraction from neighbor cells under control of Layer 3.
- Frequency hopping according to 05.02.
- Full implementation of discontinuous reception (DRX) and transmission (DTX).
- Reporting of received level and signal quality.
- Full engineering and test mode support.
- Support for all phase 1 and phase 2 handover modes.
- SIM Interface driver.
- Message interfacing to Layer 3 (Radio Resources Manager) and Layer 2 (data link layer, both signaling and data).
- External functions for AGC, AFC and synthesizer setting are called by Layer 1. These allow the user to configure the system for a wide range of radio architectures.

The higher layers of the protocol stack also reside on this embedded processor.

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD20msp415 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## POWER DISSIPATION CONSIDERATIONS

In mobile applications, minimizing the power consumption of all devices is critical to achieve longer standby and talk times. In a GSM handset the baseband subsystem dominates the current consumption of the phone in standby. The design of the GSMP and VBC includes extensive features to reduce power consumption and give standby times of up to 100 hours.

Both devices are specifically designed to operate from 2.7 V to 3.3 V, to enable three or four cell battery designs.

The GSMP incorporates intelligent power management, permitting automatic control of power consumption in the Channel Codec part of the GSMP and the peripheral circuitry. Data processing modules are switched on only when they process data, otherwise they are powered down. Additional control signals are provided that enable the Layer 1 software to control the external subsystems, such as the VBC, the radio and memory components, so that their power is intelligently switched by the GSMP.

In the VBC, the power-down functions are split separately among receive, transmit and auxiliary circuits. This provides optimal analog power performance when operating in different modes.

## INTERFACES

The chipset has eleven external interfaces (see Figure 5) that have to be considered in the design of the complete mobile radio.

- Analog Voice Interface to VBC
- Radio Interface to VBC and GSMP
- Digital SIM Card Interface to GSMP
- Digital Interface to the Keypad
- Digital Bus Interface from GSMP to Memory and Display
- Digital Audio Interface (DAI)
- Digital Interface to GSMP for Data Services
- Digital Interface from the GSMP to the EEPROM
- Digital Interface from GSMP to Accessories
- Digital Test Interface
- Digital Interface from GSMP to Optional EFR Coprocessor

### Analog Voice Interface to VBC

The analog voice interface to the VBC is specified in the AD6421 data sheet. Several design examples are given for single-ended or differential inputs or outputs. A voltage reference for biasing the microphone signal is provided on the VBC. The analog output of the VBC is capable of directly driving an earpiece with an impedance of 32 Ω. For optional use of a separate external microphone and power amplifier, a set of auxiliary input/output signals are provided on the VBC.

### Radio Interface to VBC and GSMP

The analog interface between the VBC and the radio subsystem is specified in detail in the AD6421 data sheet. The digital interface between the GSMP and the radio subsystem is specified in detail in the AD6422 data sheet.

### Digital SIM Card Interface to GSMP

The GSMP is designed to interface directly to the SIM. However, interface logic may be necessary to connect the 3 V chipset to a 5 V SIM.

### Digital Interface to Keypad

Keypad interface logic for up to 30 keys is provided on the GSMP. This interface provides keyboard scan for six rows and four columns. Additionally, an extra column can be implemented by using the "ghost column" method.

### Digital Bus Interface to Memory and Display

External RAM and ROM, as well as the display controller, interface directly to the 21-bit address bus and 16-bit data bus of the GSMP.

### Interface to FLASH Memory

The large FLASH memory can contain all programs for the embedded Control Processor of the GSMP. This includes the complete GSM protocol software as well as the User Interface Software. A total size of 8 Mbits is suggested, assuming a typical size of User Interface and a GSM Phase 2 Software. Enhanced features requiring larger memories are easily supported by the large address space of the embedded Control Processor.

To support FLASH memory, the GSMP provides embedded code to download the software into the FLASH memory via its standard serial port.

### Interface to SRAM

In addition to the FLASH memory, the Control Processor also supports static RAM to store user-defined variables, typically those used by the Protocol Stack or Application Layer. Standard SRAMs interface directly to the address and data bus of the GSMP.

### Interface to Display Controller

This interface is achieved through the address and data buses and associated read and write strobes, as well as a specific enable signal. One backlight pin with PWM control is provided by the GSMP to control brightness of backlight.

### Digital Audio Interface (DAI)

As required by the GSM specifications, a digital audio interface is provided to allow certain tests of the audio section during type approval. This interface is activated in one of the test modes. A fully functional "DAI box" needed for the FTA process may be obtained from Analog Devices upon request.

### Digital Interface to GSMP for Data Services

The chipset uses a serial interface that is connected to an external data terminal adapter as described in the AD6422 data sheet.

### Digital Interface from the GSMP to the EEPROM

The GSMP provides separate pins to interface directly to an external serial EEPROM via a serial bus. This EEPROM is typically used for storage of calibration or user variable parameters like:

- Handset Identifier (IMEI)
- Language
- Keypad Lock
- DTMF ON/OFF
- Radio Calibration Parameters

A typical size of the EEPROM is 2K × 8 bits, but this depends on the individual design of the handset.

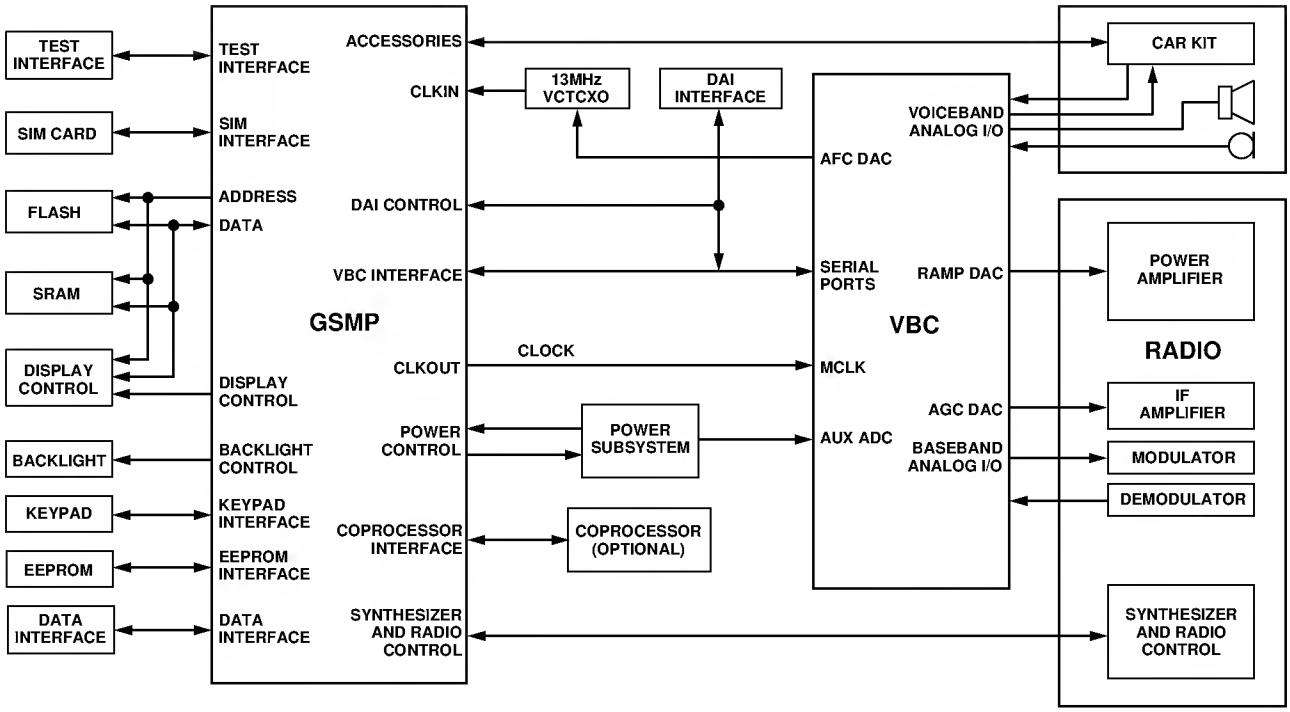


*Figure 5. Chipset Interfaces*

**Digital Interface from the GSMP to Accessories**
To allow proper control of external accessories like a car kit, the AD6422 provides a 10-pin accessory interface comprised of eight general purpose I/O channels, one chip select and one power control signal.

**Digital Test Interface**
The AD6421 and the AD6422 both support advanced test methodologies by providing JTAG Boundary Scan. Additionally, the AD6422 provides Test/Mode pins, which select different test and operating modes.

**Digital Interface from GSMP to Optional EFR-Coprocessor**
The AD6422 provides a digital interface to an external EFR Coprocessor (DSP). This coprocessor is required to handle the Enhanced Full Rate speech codec in PCS1900 mobile radios.

**Baseband Processing Key Parts List**
Table I lists the major hardware components necessary to complete the GSM baseband processing subsystem.

**Table I. List of Key Components**

| Description | Specification |
|---|---|
| GSMP[1] | AD6422 |
| VBC[1] | AD6421 |
| EFR-Coprocessor[2] | AD6423 |
| FLASH[3] | 256K × 16, 150 ns |
| SRAM | 128K × 8, 120 ns |
| EEPROM[4] | 2K × 8 |
| Display Driver | Design Specific |

NOTES
[1]These components comprise the AD20msp415 chipset.
[2]The EFR-Coprocessor is required only in systems requiring support of the Enhanced Full Rate speech codec.
[3]A size of 4 Mbits is recommended to allow storage of all GSM Layer (1, 2, 3) programs for GSM Phase 2 as well as a typical User Interface (MMI).
[4]Can be omitted if parameters are stored in FLASH memory.

## MECHANICAL CONSIDERATIONS

The chipset has been specifically designed to meet not only cost and power consumption requirements but also the physical dimensions. State-of-the-art package technology was used to achieve the smallest possible geometries. (See Table II for list of packaging dimensions and consult individual data sheets of the two components for further details.)

**Table II. Package Dimensions**

| Parameter | GSMP | VBC | EFR* | Unit |
|---|---|---|---|---|
| Package | TQFP | TQFP | TQFP | |
| Leads | 144 | 64 | 64 | # |
| Pitch | 0.5 | 0.5 | 0.5 | mm |
| Body | 20 × 20 | 10 × 10 | 10 × 10 | $mm^2$ |
| Total Height | 1.6 | 1.6 | 1.6 | mm |
| Board Area | 22 × 22 | 12 × 12 | 12 × 12 | $mm^2$ |

*The EFR Coprocessor is needed only in systems requiring support of Enhanced Full Rate Speech Codec.

All components use low profile Plastic Quad Flatpacks with lead pitches of 0.5 mm, for PCMCIA applications.

## ORDERING GUIDE

| Part Number | Supply Voltage Range |
|---|---|
| AD6421AST | +2.7 V to +3.3 V |
| AD6422AST | +2.7 V to +3.3 V |
| AD6423 | +2.7 V to +3.3 V |

An Evaluation and Development system may be ordered for this chipset, under the part number, NRE20msp415EB1.

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